

## CLAIMS

What is claimed is:

1. A binary search method for suppressing a carrier in a quadrature modulator, comprising:

applying a set of four correction signal pairs to a quadrature modulator and

detecting a first set of four output signals;

identifying an optimum correction signal pair from among the set of four

correction signal pairs;

using the optimum correction signal pair to determine another set of four

correction signal pairs;

repeating the applying, identifying, and using steps for a predetermined

number of times to produce a final correction signal pair; and

using the final correction signal pair to suppress a carrier in the quadrature modulator.

2. The binary search method of claim 1, further comprising creating a search area, the search area having a set of four search area quadrants.

3. The binary search method of claim 2, wherein each of the set of four correction signal pairs corresponds to a center of a respective search area quadrant.

4. The binary search method of claim 2, wherein creating the search area

comprises determining a maximum DC offset.

5. The binary search method of claim 4, wherein creating the search area comprises creating a step as a function of the maximum DC offset.

6. The binary search method of claim 2, wherein creating the search area comprises creating an unrotated search area.

7. The binary search method of claim 2, wherein creating the search area comprises creating a rotated search area.

8. The binary search method of claim 1, wherein identifying the optimum correction signal pair comprises identifying a correction signal pair that yields the smallest output signal.

9. The binary search method of claim 1, wherein applying the optimum correction signal pair to the quadrature modulator comprises applying a signal of the first optimum correction signal pair to an in-phase channel and applying a second signal of the optimum correction signal pair to a quadrature-phase channel.

10. A program storage device, readable by a machine and tangibly embodying a representation of a program of instructions adapted to be executed by said machine to perform the method of claim 1.

11. A method for suppressing a carrier in a quadrature modulator, comprising:
  - performing a search method to determine a pair of receiver path correction signals;
  - performing the search method to determine a pair of transmitter path correction signals; and
  - using the pairs of receiver path and transmitter path correction signals to suppress a carrier signal in a quadrature modulator.
12. The method of claim 11, where using the pairs of receiver path and transmitter path correction signals comprises:
  - subtracting a first receiver path correction signal from a first downconverter output;
  - subtracting a second receiver path correction signal from a second downconverter output;
  - subtracting a first transmitter path correction signal from a first upconverter input; and
  - subtracting a second transmitter path correction signal from a second upconverter input.
13. The method of claim 11, where performing the search method includes performing a binary search method.
14. The method of claim 11, further comprising operating the quadrature modulator.

15. A program storage device, readable by a machine and tangibly embodying a representation of a program of instructions adapted to be executed by said machine to perform the method of claim 11.

16. A method for suppressing a carrier in a quadrature modulator, comprising:  
performing a calibration method to determine a pair of receiver path correction signals;  
performing a search method to determine a pair of transmitter path correction signals; and  
using the pairs of receiver path and transmitter path correction signals to suppress a carrier signal in a quadrature modulator.

17. The method of claim 16, where using the pairs of receiver path and transmitter path correction signals comprises:  
subtracting a first receiver path correction signal from a first downconverter output;  
subtracting a second receiver path correction signal from a second downconverter output;  
subtracting a first transmitter path correction signal from a first upconverter input; and  
subtracting a second transmitter path correction signal from a second upconverter input.

18. The method of claim 16, where performing the calibration method includes performing a feedback DC calibration method.

19. The method of claim 16, where performing the search method includes performing a binary search method.

20. The method of claim 16, further comprising operating the quadrature modulator.

21. A program storage device, readable by a machine and tangibly embodying a representation of a program of instructions adapted to be executed by said machine to perform the method of claim 16.

22. An apparatus for suppressing a carrier in a quadrature modulator, comprising:  
a first pair of summers;  
an upconverter circuit coupled to the first pair of summers, each of the pair of summers being coupled to a quadrature channel;  
a multiplexer coupled to the upconverter circuit, to a ground, and to an RF front end;  
a downconverter circuit coupled to the multiplexer;  
a second pair of summers coupled to the downconverter circuit, each of the pair of summers being coupled to a quadrature channel; and  
a correction circuit coupled to the first and second pairs of summers, the correction circuit performing a first correction method to determine a

pair of receiver path correction signals, performing a second correction method to determine a pair of transmitter path correction signals, and using the pairs of receiver path and transmitter path correction signals to suppress a carrier signal in a quadrature modulator.

23. The apparatus of claim 22, the correction circuit further comprising:
  - a pair of averaging circuits coupled to the first pair of summers;
  - a pair of absolute value circuits coupled to the pair of averaging circuits;
  - a summer coupled to the pair of absolute value circuits; and
  - a search circuit coupled to the summer.
24. The apparatus of claim 22, the search circuit comprising a binary search circuit.
25. The apparatus of claim 22, further comprising a feedback DC calibration circuit coupled to the pair of averaging circuits.
26. The apparatus of claim 22, further comprising a control circuit coupled to the correction circuit and to the multiplexer.
27. The apparatus of claim 22, further comprising a program storage device coupled to the control circuit.

28. An integrated circuit for suppressing a carrier in a quadrature modulator comprising the apparatus of claim 22.